ABSTRACT OF THE DISCLOSURE

A self aligned method of forming an array of floating gate memory cells, and an array formed thereby, wherein each memory cell includes a trench formed into a surface of a semiconductor substrate, and spaced apart source and drain regions with a channel region formed therebetween. The drain region is formed underneath the trench. An electrically conductive floating gate is formed over and insulated from a portion of the channel region, with a horizontally oriented edge extending therefrom. An electrically conductive control gate is formed having a first portion disposed in the trench and a second portion disposed adjacent to and insulated from the floating gate edge.